Specifications

Table 32 lists the specifications for the A/D subsystem.

Table 32: A/D Subsystem Specifications

Feature	DT9801/-EC/-EC-I, DT9802/-EC/-EC-I Specifications	DT9803/-EC/-EC-I, DT9804/-EC/-EC-I, DT9805, DT9806 Specifications
Number of analog inputs Single-ended/ pseudo-differential: Differential:	 16 8	 16 8 (7 thermocouple inputs, 1 CJC on DT9805/06)
Number of gains	4 (1, 2, 4, 8)	4 (1, 2, 4, and 8 for DT9803/04; 1, 10, 100, 500 for DT9805/06)
Resolution	12 bits	16 bits
Data encoding	Offset binary	
Coupling	DC	
Over voltage protection Off: On:	 ±25 V ±40 V	
ESD protection	1.5 kV	
System Error	0.03% FSR	0.01% FSR

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Table 32: A/D Subsystem Specifications (cont.)

Feature	DT9801/-EC/-EC-I, DT9802/-EC/-EC-I Specifications	DT9803/-EC/-EC-I, DT9804/-EC/-EC-I, DT9805, DT9806 Specifications
System accuracy (full-scale) Gain = 1: Gain = 2: Gain = 4: Gain = 8: (DT9805/9806 only) Gain = 10: Gain = 100: Gain = 500:	 0.03% 0.04% 0.05% 0.05%	 0.01% 0.02% 0.03% 0.03% 0.02% 0.03% 0.04%
Nonlinearity (integral)	±1.0 LSBs	±4.0 LSBs
Differential linearity	±0.5 LSBs (no missing codes)	±1.0 LSBs (no missing codes) for DT9803/04 ±1.2 LSBs (no missing codes) for DT9805/06
Range	0 to 1.25 V, 2.5 V, 5 V, 10 V ±1.25, 2.5, 5, 10 V	±1.25 V, 2.5 V, 5 V, 10 V for DT9803/04 ±0.020 V, 0.10 V, 1 V, 10 V for DT9805/06
Drift Zero: Gain:	 ±30 µV+ (+20 µV * Gain)/° C ±30 ppm/° C	 ±25 µV+ (+10 µV * Gain)/° C for DT9803/04 [a] ±25 µV+ (+5 µV * Gain)/° C for DT9805/06 ±20 ppm/° C

Table 32: A/D Subsystem Specifications (cont.)

Feature	DT9801/-EC/-EC-I, DT9802/-EC/-EC-I Specifications	DT9803/-EC/-EC-I, DT9804/-EC/-EC-I, DT9805, DT9806 Specifications
Input impedance Off: On:	100 MΩ, 10 pF[b] 100 MΩ, 100 pF[b]	
Channel-gain list	32 Samples	
Internal reference	+2.5 V ±0.002 V	
Input bias current	±20 nA	±20 nA for DT9803/04 +250 nA for DT9805/06[c] (Ch1-7) ±10 nA for DT9805/06 (Ch8-15)
Common mode voltage	±11 V maximum (operational)	
Maximum input voltage	±40 V maximum (protection)	
A/D converter noise	0.3 LSB rms	0.4 LSB rms
Amplifier input noise	20 µV rms + (10 µV rms * gain) 200 pA rms (current)	15 µV rms + (10 µV rms * gain) 100 pA rms (current)
Channel-to-channel offset	±40 µV	±40 µV
Channel acquisition time	3 µs	5 µs for DT9803/04 6 µs (Gain = 1) for DT9805/06 250 µs (Gain = 500) for DT9805/06

Table 32: A/D Subsystem Specifications (cont.)

Feature	DT9801/-EC/-EC-I, DT9802/-EC/-EC-I Specifications	DT9803/-EC/-EC-I, DT9804/-EC/-EC-I, DT9805, DT9806 Specifications
A/D conversion time	6.6 µs	8 µs
Effective number of bits (ENOB) at 1 kHz input	11.5 bits	13.5 bits for DT9803/04 14.1 bits for DT9805/06
Total Harmonic Distortion	–80 dB typical	–90 dB typical
Channel crosstalk	–80 dB @ 1 kHz	
Minimum Data Throughput (Internal Clock)	0.75 S/s	
Data throughput Single analog channel:	100 kSamples/s (0.03% accuracy)	100 kSamples/s for DT9803/04 (0.01% accuracy); 50 kSamples/s for DT9805/06 (0.01% accuracy)
Multiple channels (scan with gain of 1 to 10):	100 kSamples/s (0.03% accuracy)	100 kSamples/s for DT9803/04 (0.01% accuracy); 50 kSamples/s for DT9805/06 (0.01% accuracy)
Multiple channels (scan with gain of 100):	–	10 kSamples/s (0.03% accuracy)

Table 32: A/D Subsystem Specifications (cont.)

Feature	DT9801/-EC/-EC-I, DT9802/-EC/-EC-I Specifications	DT9803/-EC/-EC-I, DT9804/-EC/-EC-I, DT9805, DT9806 Specifications
Data throughput (cont.) Multiple channels (scan with gain of 500): Single digital channel:	– 100 kSamples/s	2 kSamples/s (0.04% accuracy) 100 kSamples/s for DT9803/04; 50 kSamples/s for DT9805/06
CJC Voltage @ 25° C	–	+0.250 V
Cold Junction Accuracy	–	+1° from 5° to 45° C
Break Detection Current[d]	–	+250 nA (high side differential)
External A/D sample clock Input type High-level input voltage: Low-level input voltage: Minimum pulse width: Maximum frequency:	 HCT Rising-Edge Sensitive with 22 kΩ pull-up resistor 2.4 V minimum 0.8 V maximum 600 ns (high); 600 ns (low) 750.0 kHz	

Table 32: A/D Subsystem Specifications (cont.)

Feature	DT9801/-EC/-EC-I, DT9802/-EC/-EC-I Specifications	DT9803/-EC/-EC-I, DT9804/-EC/-EC-I, DT9805, DT9806 Specifications
External A/D digital (TTL) trigger		
Input type	HCT Rising-Edge Sensitive with 22 kΩ pull-up resistor	
High-level input voltage:	2.4 V minimum	
Low-level input voltage:	0.8 V maximum	
Minimum pulse width:	600 ns (high); 600 ns (low)	
Maximum frequency:	750.0 kHz	
Dynamic Digital Output		
Output driver:	TTL	
Output driver high voltage:	2.4 V maximum (IOH = 1 mA)	
Output driver low voltage:	0.5 V maximum (IOL = 2 mA)	
Back EMF Diodes	Yes	

a. This value is referenced to voltage entering the A/D converter. To reference this value to the original voltage signal, use {[+/-25 + (5uV * Gain)] / Gain} / degrees C.
b. On channel 0 only on the DT9805 and DT9806 modules, the input impedance is 10 kΩ.
c. Break detection current.
d. Broken thermocouples in differential mode will output plus full scale for gains equal to or greater than 10.

Table 33 lists the specifications for the D/A subsystem.

Table 33: D/A Subsystem Specifications

Feature	DT9802/-EC/-EC-I Specifications	DT9804/-EC/-EC-I, DT9806 Specifications
Number of analog output channels	2	
Resolution	12 bits	16 bits
Data encoding (input)	Offset binary	
Nonlinearity (integral)	±1 LSBs	±4 LSBs
Differential linearity	±0.5 LSBs (monotonic)	±1.0 LSB (monotonic)
Output range	0 to 5 V, 10 V ±5 V, 10 V	±10 V
Zero error	Software-adjustable to zero	
Gain error	±2 LSBs	±6 LSBs
Current output	±5 mA minimum (10 V/ 2 kΩ)	
Output impedance	0.3 Ω typical	
Capacitive drive capability	0.001 µF minimum (no oscillations)	
Protection	Short circuit to Analog Common	
Power-on voltage	0 V ±10 mV maximum	
Settling time to 0.01% of FSR	50 µs, 20 V step; 10 µs, 100 mV step	
Throughput (Full Scale)	Single value (system dependent)	
Slew rate	2 V/µs	

Table 34 lists the specifications for the digital input subsystem.

Table 34: DIN Subsystem Specifications

Feature	Specifications
Number of lines	8 (Port A)
Termination	None
Inputs Input type: Input load: High-level input voltage: Low-level input voltage: High-level input current: Low-level input current:	 Level sensitive 1 (HCT) 2.0 V minimum 0.8 V maximum 3 µA –3 µA
Maximum internal pacer rate (single digital channel)[a]	Maximum A/D throughput of the board
Back EMF diodes	No

a. This digital channel must be the only channel included as part of the channel list.

Table 35 lists the specifications for the digital output subsystem.

Table 35: DOUT Subsystem Specifications

Feature	Specifications
Number of lines	8 (Port B)
Termination	22 kΩ resistor
Outputs Output driver: Output driver high voltage (source): Output driver low voltage (sink):	 74HCT244 (TTL) 2.4 V minimum (IOH = 1 mA) 0.5 V maximum (IOL = 12 mA)
Back EMF diodes	Yes

Table 36 lists the specifications for the C/T subsystems.

Table 36: C/T Subsystem Specifications

Feature	Specifications
Number of counter/timer channels	2
Clock Inputs Input type: High-level input voltage: Low-level input voltage: Minimum pulse width: Maximum frequency:	 HCT with 22 kΩ pull-up resistor 2.4 V minimum 0.8 V maximum 600 ns (high); 600 ns (low) 750 kHz
Gate Inputs Input type: High-level input voltage: Low-level input voltage: Minimum pulse width:	 HCT with 22 kΩ pull-up resistor 2.4 V minimum 0.8 V maximum 600 ns (high); 600 ns (low)
Counter Outputs Output driver high voltage: Output driver low voltage:	 3.0 V minimum @ 1 mA Source 0.4 V maximum @ 2 mA Sink

Table 37 lists the power, physical, and environmental specifications for the DT9800 Series modules.

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Table 37: Power, Physical, and Environmental Specifications

Feature	Specifications
Power	
+5 V Standby:	0.5 µA maximum
+5 V Enumeration:	100 mA maximum
+5 V Power ON:	500 mA maximum
+5 V Isolated Power Out (TB27)	10 mA maximum
Physical	
Dimensions:	
DT9800 Standard Series:	6.5 inches x 4.5 inches x 1.4 inches
DT9800-EC and DT9800-EC-I Series	7.42 inches x 3.40 x 0.736 inches
Weight:	9 ounces (255 grams)
Environmental	
Operating temperature range:	0° C to 55° C
Storage temperature range:	–25° C to 85° C
Relative humidity:	To 95%, noncondensing

Table 38 lists the screw terminal and cable specifications for the DT9800 Standard modules.

Table 38: DT9800 Standard Cable and Terminal Block Specifications

Feature	Specifications
Recommended cable	2-meter, Type A-B, USB cable AMP part 1487588-3
Screw terminal block (TB1-TB6)	9-Position Header: PCD, Inc. part ELVH09100 Mating plug: PCD, Inc. part ELVP09100

Table 39 lists the connector specifications for the DT9800-EC and DT9800-EC-I Series modules.

Table 39: DT9800-EC/EC-I Connector Specifications

Feature	Header	Mating Cable Connector
26-pin connector (J5, J6)	AMP/Tyco part 1761686-9	AMP/Tyco part 1658622-6
50 pin connector (J4)	AMP/Tyco part 1-1761686-5	AMP/Tyco part 1-1658622-0

Table 40 lists the regulatory specifications for the DT9800 Series modules.

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Table 40: Regulatory Specifications

Feature	Specifications
Emissions (EMI)	FCC Part 15, EN55022:1994 + A1:1995 + A2:1997 VCCI, AS/NZS 3548 Class A
Immunity	EN61000-6-1:2001
RoHS (EU Directive 2002/95/EG)	Compliant (as of July 1st, 2006)